

A NOVEL 3V, 7 mA PHEMT GaAs ACTIVE MMIC MIXER/LNA FOR WIRELESS APPLICATIONS.

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ABSTRACT

A novel monolithic integrated active Mixer/LNA utilizing advanced pseudomorphic GaAs FETs has been developed. RF Frequency coverage is 900 MHz to 2400 MHz. The Mixer/LNA operates on a single 3 Volt supply at 7 mA. The mixer provides 4 dB conversion gain with a -10 dBm LO drive. The LNA provides a 1.6 dB noise figure and 14 dB gain. The die is small packaged in the SSOP-16 plastic package to keep costs low. This is the only GaAs PHEMT active Mixer/LNA known to provide such performance from such a small DC requirement.

INTRODUCTION

Consumers today expect cordless and cellular wireless systems to provide hours of talk time and yet be easily carried around. Manufacturers are being driven to produce smaller, more efficient, less expensive solutions. An area in research and development is the front RF receiver mixing and low noise amplification functions.

The Mixer/LNA MMIC described in this paper is designed to provide a cost effective monolithic solution for a wireless RF receiver. The Mixer/LNA low noise amplifies, then downconverts, a received RF signal (900 to 2400 MHz) to the IF frequency (50 to 300 MHz). An external filter is inserted between the LNA and mixer to provide image rejection. A built in LO buffer amplifier lowers external oscillator requirements to at least -10 dBm of delivered power. External matching is required for all Mixer and LNA ports at the specific frequency of interest. The Mixer/LNA operates on a single 3.0 Volt supply and 7.0 mA. The MMIC is prototyped in a surface mount SSOP-16 and SC-70 plastic packages.

This paper describes the fabrication and models used to develop this monolithic design. The design, package, and application are discussed. Finally, measured results are shown.

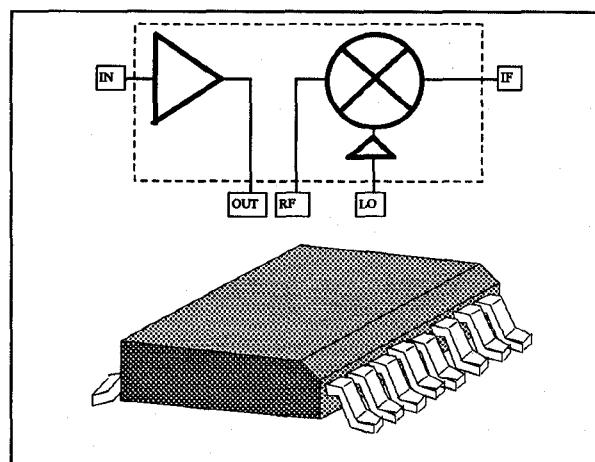


Fig. 1 A GaAs PHEMT Mixer/LNA.

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DEVICE AND FABRICATION

The devices used in this monolithic design were pseudomorphic high electron mobility transistor (PHEMT) structures built using molecular beam epitaxy (MBE) material growth techniques. The gates were defined using electron-beam lithography. Gate lengths range from 0.12 to 0.17 microns. The remaining layers are placed on the 3-inch wafers using precision steppers. The result is a process with typical F_T of 60 GHz and able to operate utilizing very low voltage and current density.

The design's primary active device consists of an interdigitated FET structure ranging from $25\mu\text{m}$ to $300\mu\text{m}$ periphery. The typical DC characteristics of these devices are an $Idss$ of 0.35A/mm with a pinch off voltage of -0.5V and a transconductance of 330 mS/mm . Silicon nitride is used for passivation and MIM capacitors. Resistors are built using the natural 300 ohms/square bulk active material resistance. From measured on wafer I-V curves and s-parameters, a Statz small signal equivalent model was constructed as shown in Figure 2.

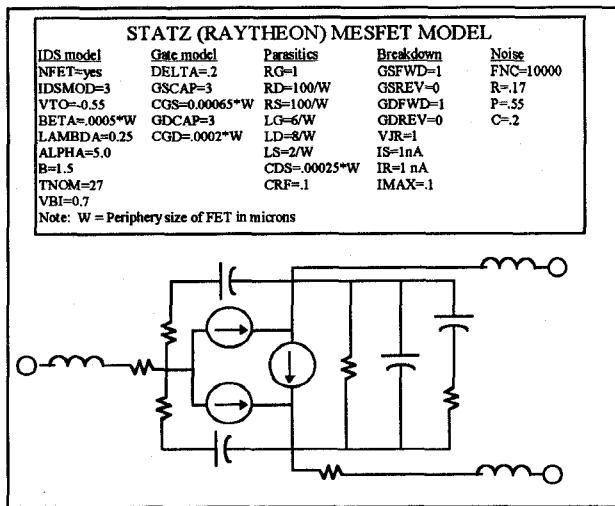


Fig. 2. PHEMT equivalent FET circuit model.

MONOLITHIC MIXER/LNA DESIGN

Performance goals for the low cost Mixer/LNA were 3 volt operation with 6 to 8 mA current, 20 dB total gain, 3 dB noise figure, and at least a -20 dBm input IP3. A GaAs PHEMT process was selected for its excellent gain and noise figure performance at low DC levels. Since the process is inherently more expensive than Silicon or regular GaAs, it was paramount that the design consume the least amount of die area. A dual gate FET type architecture was selected for mixing because of its compact size. A LO buffer amp. was incorporated to reduce LO drive. Last, a feedback common source - source follower amplifier is used for its stability, low noise, and copious gain. All design were simulated on Hewlett-Packard's HP85150B Microwave Design System (MDS) on a HP 735 workstation.

The active FET mixer used in the HP design is cascode in nature. The actual monolithic implementation is a two series FET design. Such a design offers isolation between RF and LO ports equivalent to a balanced diode design. The topology also offers conversion gain, small size, and can be monolithically implemented. While the dual gate mixer is not novel, this implementation is unique.

Figure 3 shows the mixer schematic. Since a dual-gate FET mixer utilizes transconductance mixing, the lower LO FET is made large to maximize the transconductance range. The upper RF FET is optimized to provide maximum gain. A current source and source capacitor combination are used to elevate the dual-gate FET source node to pinch-off the FET to a specific percentage of Idss. The LO and RF ports are tied to ground through resistors. DC current is thus regulated to 3 mA when

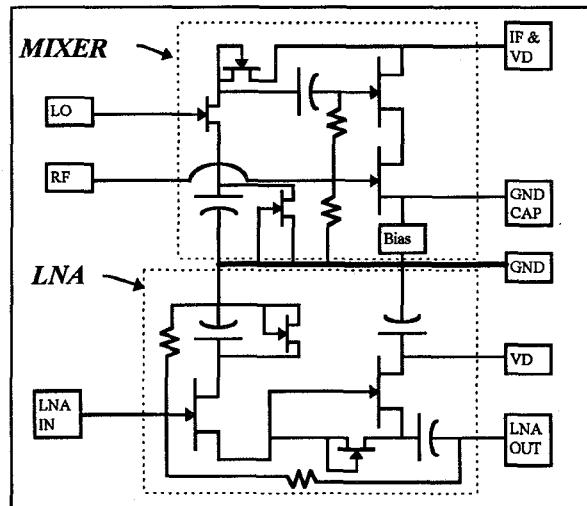


Fig. 3. Schematic Mixer/LNA.

voltage applied to the dual-gate drain is 3 volts.

One of the problems with traditional dual-gate designs is that LO drive power tends to be higher than most applications can provide. An external oscillator buffer amplifier is expensive and consumes valuable DC power. The mixer takes advantage of the fact that the LO port is voltage driven and is a high impedance. A simple LO buffer amplifier is incorporated into the design to provide voltage amplification. The amplifier converts the 50 Ohm LO input into the much higher LO impedance with little power gain but much voltage gain, at a cost of only 1.0 mA. The buffer amplifier also utilizes current sources to set bias and provide RF isolation.

Figure 3 also shows the MMIC LNA. This two stage design incorporates feedback from output to input. The first stage is a common source FET that provides the primary gain for the MMIC. The second stage is a source follower that is used for impedance match, bias, and a feedback path. Current is shared by both stages and regulated to 3.0 mA with the use of current sources.

The Mixer/LNA is unique in the fact that there is zero volts DC at the RF, LO, LNA input and LNA output ports. This allows easy cascading and matching. The design is insensitive to DC variation with allowing operation over a 2.7V to 5.5V power supply range. The Mixer/LNA is intentionally left partially matched at all high frequency ports (RF, LO, LNA) since matching would increase cost (more MMIC die area) and reduce flexibility. External matching allows the user to configure the match for the preferred frequency and selectivity. Also, high Q external components allow very narrow band match for best image rejection and return loss.

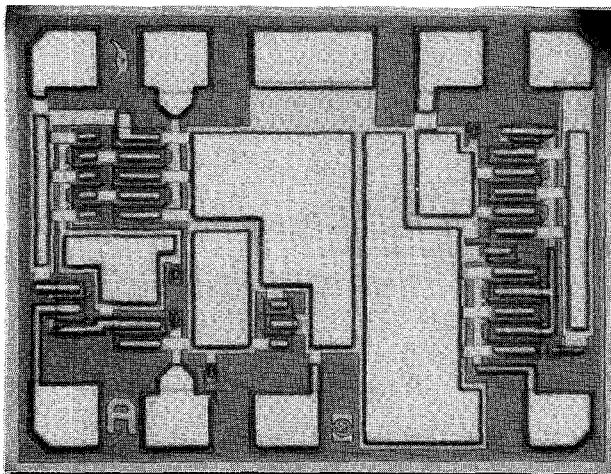


Fig 4. Micro-photograph of the Mixer/LNA MMIC.

Figure 4 shows a Mixer/LNA MMIC photograph. Die size is 0.56 by 0.71 mm resulting in approximately 10,000 die per wafer. Separate DC and RF ground are used to conserve die area.

PACKAGING

Two plastic package options were used for the Mixer/LNA. The first option is a SSOP-16 package. The second option is to fabricate the Mixer and LNA separate and house each in a SC-70 package. While the SSOP-16 option is a cleaner solution, the separate mixer and LNA in SC-70 approach offers less common lead ground problems (better isolation) and lower parasitics. The SSOP-16 occupies 30 sq. mm. while two SC-70 parts only occupy 12 sq. mm. of printed circuit board space. Figure 5 shows each package pin out designation.

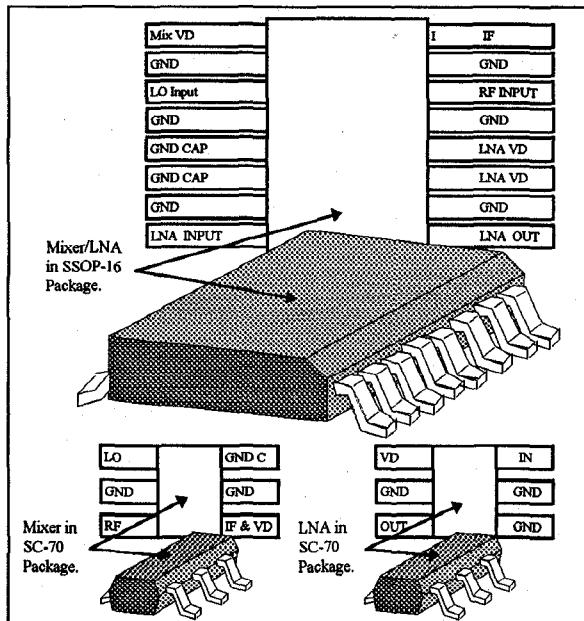


Fig 5. Mixer/LNA in SSOP-16 and SC-70.

IMPEDANCE MATCHING AND RESULTS

Since the Mixer/LNA must be externally matched for the specific frequency of application, three frequency systems were built and tested to demonstrate performance. Selected commercial frequencies were Cellular (RF=880 MHz, LO=950 MHz), DECT (RF=1890 MHz, LO=1780 MHz), and ISM (RF=2400 MHz, LO=2200 MHz).

The Mixer requires matching on all ports. The RF port requires a series C (.5-6 pF) and shunt L (1-13 nH). This high pass patch allows good RF return loss while terminating the IF leakage to ground. The LO port is a simple series L (1-8 nH) to match the buffer amplifier. The IF port has a series L (15-30 nH) and DC block C (1000 pF) for low pass filtering. In addition a 4:1 transformer is used to convert the 200 Ω IF output impedance to 50 Ω . The DC is brought in through a low Q choke.

The LNA section also requires impedance matching. The input is partial matched to 50 Ω through the use of feedback. With a simple series L (.5-6 nH) and shunt L (0-15 nH) the input can be matched to I_{opt} (minimum noise). The output is matched to 50 Ω above 2 GHz. Below 2 GHz a series L (.5-1 nH) match can be used.

Figure 6 shows an example of a typical application utilizing the Mixer/LNA. In such a system with a Mixer/LNA, image rejection filter (2 dB loss), and external matching components, a 19 dB gain and 3 dB noise figure can typically be measured. The input 3rd order intercept point is -19 dBm (output -2 dBm). The LNA input to LO input isolation is 17 dB (28 dB in SC-70). LO input to IF output isolation is about 25 dB. Average current is 7 mA with 3V applied. See Table 1 for typical overall performance results and Table 2 for measured results at the three test frequencies.

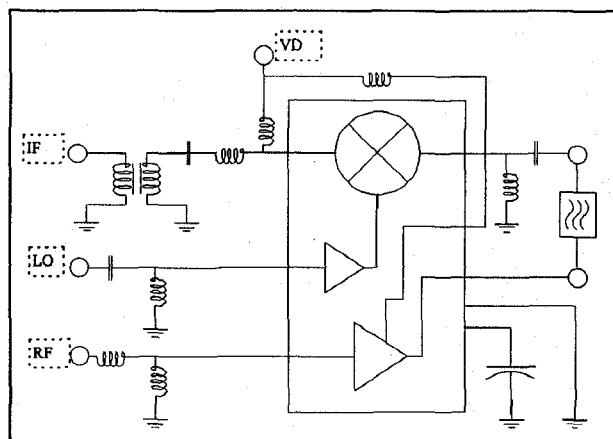


Fig. 6 Mixer/LNA as tested.

Parameter	Typical	Unit
RF Input Freq. Range	900 - 2400	MHz
LO Input Freq. Range	500 - 3000	MHz
IF Frequency Range	50 - 550	MHz
Mixer/ LNA total Gain	19	dB
Mixer/ LNA Noise Figure	3.2	dB
LNA to RF Isolation	17	dB
LO to IF Isolation	25	dB
Mixer / LNA P-1dB	-9	dBm
Output Third Order Int.	-1.9	dBm
Minimum LO Drive Level	-10	dBm
DC Power Voltage	3	Volt
DC Current Level	7.0	mA

Table 1. Typical MMIC Mixer/LNA performance.

Parameter	900 MHz	1.8 GHz	2.4 GHz
Mixer Conv Gain	4.4 dB	4.8 dB	3.2 dB
Mixer N. F.	10.2 dB	10.5 dB	11 dB
RF Return Loss	-11.6 dB	-21 dB	-15 dB
LO Return Loss	-8.5 dB	-12 dB	-13 dB
IF Return Loss	-16 dB	-15 dB	-12 dB
LO to IF Isolation	16 dB	33 dB	35 dB
RF to IF Isolation	13 dB	22 dB	24 dB
Mixer P-1dB	-7.5 dBm	-9 dBm	-10 dBm
Mixer output IP3	-2.0 dBm	-1.5 dBm	-2.0 dBm
LNA Noise Figure	1.9 dB	1.55 dB	1.6 dB
LNA Gain	15 dB	14.2 dB	12.5 dB
IN Return Loss	-10 dB	-11 dB	-12 dB
OUT Return Loss	-9.5 dB	-10 dB	-15 dB
LNA P-1dB	-1.2 dBm	-1.5 dBm	-2 dBm
LNA Output IP3	+8 dBm	+8.5 dBm	+8 dBm

Table 2. Measured Mixer and LNA performance.

SUMMARY

A Mixer/LNA MMIC based on PHEMT FETs and fabricated on MBE GaAs material with stepper lithography and electron beam written gates has been demonstrated. Such a process is traditionally reserved for high performance, expensive devices. However, when MMIC size is kept small, yields high, and standard plastic packages used a PHEMT MMIC can be manufactured for low cost. The PHEMT devices provide low noise, very high gain, and good linearity while operating at very low voltages and currents. These characteristics are ideal for an active low DC power Mixer/LNA.

The final mixer design is compact and efficient. The chip size is 0.4 sq. mm., easily fitting into the SSOP-16 package. The LNA provides 1.6 dB noise figure and 14 dB gain. The mixer provides 4 dB conversion gain and requires only a -10 dBm LO. Combined Mixer/LNA performance is 19 dB gain, 3 dB N.F. and 3.0 V, 7mA operation. This performance is across the commercial wireless bands from 900 to 2400 MHz.

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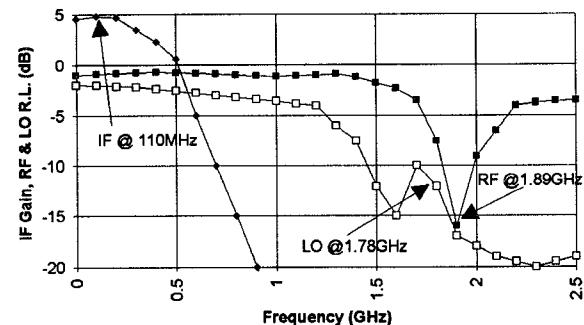


Fig. 7 Mixer IF gain, LO and RF R.L. for DECT.

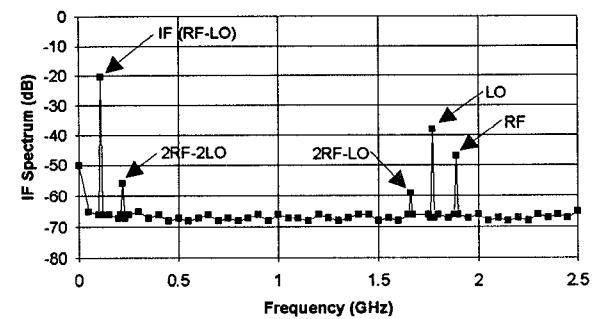


Fig. 8 Mixer IF spectrum output for DECT

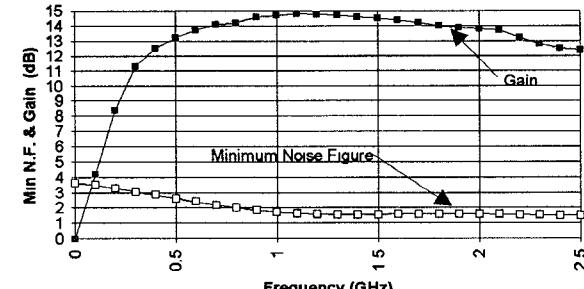


Fig. 9. LNA noise figure and associated gain.

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